# Lab 3: Simulate an ALU

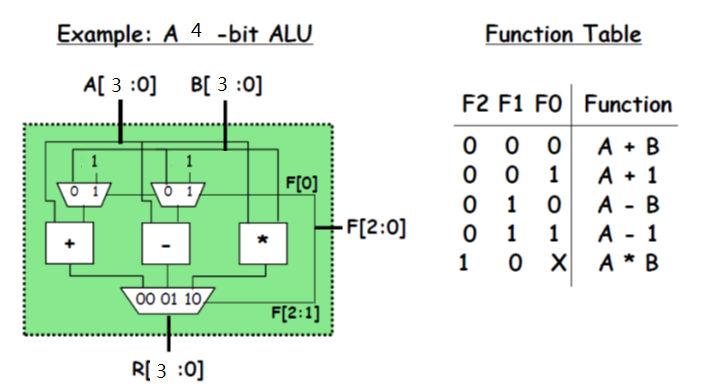
(2+2 hours)

## Goal

To learn how to write Verilog testbench to simulate the ALU designed in Lab 3.

## Procedure

Simulate the ALU with the following functions.



1. Simulate the 3-1 mux module by writing a 3-1 mux testbench, then check whether the output is correct.
2. Simulate the subtract module by writing a subtract testbench, then check whether the output is correct.
3. Simulate the ALU module by writing an ALU testbench, then check whether all the function works correctly.